--(2) Command bit block 45

This is a bit block that is received in consonance with an arbitrary timing during the blanking period. The header 41, which represents a command bit block, is [1100]. Each source driver IC 20 (Fig. 1) interprets the control data contained in the data 42, and drives the liquid crystal cell 2. Example control data are as follows.

(a) Start of transmission for video data

[0000-0000-0000-0000-0000-0000]

This command is used to provide notification that video data transmission has begun. After this command is issued, the transmission of video data using a data bit block, which will be described later, is initiated.

(b) Start of transmission of gamma data

[1000-1000-1000-1000-1000-1000]

This command is used to provide notification that the transmission of gamma compensation data (value for generating a reference voltage) has begun. After this command is issued, the transmission of gamma data using a data bit block, which will be described later, is initiated.

(c) Strobe ON/OFF

Strobe ON [1101-1101-1101-1101-1101-1101]

Strobe OFF [1100-1100-1100-1100-1100-1100]

These commands are used to provide notification that output to the liquid crystal cell 2 (Fig. 1) has begun. Upon the receipt of the command strobe ON, the driver controller 29 sets a strobe (STB) signal, which is to be transmitted to the LCD source driver 31, High. While upon the receipt of the command strobe OFF, the driver controller 29 sets a strobe (STB) signal, which is

to be transmitted to the LCD source driver 31, Low. Thus, during a period wherein the strobe signal is High, the output to the liquid crystal cell 2 can be maintained in a high impedance state.

(d) Designation of output polarity

Positive polarity output [1111-1111-1111-1111-1111-1111]

Negative polarity output [1110-1110-1110-1110-1110-1110]

These commands are used to designate the polarity of a voltage output to the liquid crystal cell 2. Upon the receipt of one of these commands, the driver controller 29 (Fig. 3) will set or reset an internal polarity control signal (POL).

(3) Data bit block 46

This is a bit block used for the transmission of video data or of gamma compensation data. The header 41 is [1110] and represents a data bit block, while the contents of the block are identified by using a command that was previously transmitted.

(a) Video data [Red 8-bit] [Green 8-bit] [Blue 8-bit]

The video data for one line are transmitted sequentially. For the XGA, 1024 data bit blocks 46 are sequentially received. The driver 29 for each source driver IC 20 (Fig. 1) receives only its own, individual data, and while it does this, it replaces the data bit block 46 with a wait bit block (which will be described later), and transmits the wait bit block to the succeeding source driver IC 20.

(b) Gamma compensation data [Gamma 10-bit][00000000000000]

This is a case where a reference gamma compensation voltage having a 10-bit precision is generated, for the gamma compensation the required number of data sets are transmitted. The

drivers 29 of all the source driver ICs 20 may either receive the same data, or may receive different data.

(4) Wait bit block 47

A1

This is used only by the source driver ICs 20 (Fig. 1). The header 41 is [1111] (wait) and represents a wait bit block. During the reception of video data, each source driver IC 20 transmits a wait bit block 47 to a succeeding source driver IC 20. During the reception of the wait bit block 47, the source driver IC 20 does not perform any process, and waits to receive the video data that is included in the data bit block 46.

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Page 14, line 24 to Page 15, line 8, revise to read as follows:

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A2

Fig. 5B is a diagram showing the transmission of n-line video data by using the input of a first chip that is the first source driver IC 20 and the input of a second chip that is the next source driver IC 20. After the blanking period (Sync: synchronization period), the video data transmission start command in the command bit block 45 is received, and then video data for one line is received. Subsequently, the strobe ON command is received at an appropriate time. At this time, the source driver IC 20 starts writing data to the liquid crystal cell 2 (Fig. 1). Actually, a voltage is applied to the liquid crystal cell 2 when the strobe OFF command is next received, and until that time, the output is maintained in a high impedance state. Positive output is selected by the output polarity designation command that is issued between the strobe ON command and the strobe OFF command. During the reception of its own, individual video data, the first chip in the upper portion in Fig. 5B transmits the wait bit block 47 to a succeeding

source driver IC 20 (a second chip). The second chip in the lower portion skips the wait bit block 47, starts reception of the video data, and writes data to the liquid crystal cell 2.

Page 19, line 23 to Page 20, line 4, revise to read as follows:

Figs. 13a and 13b are diagrams showing the process for generating a control signal (waveforms and the shifting of the state of each control signal). In Fig. 13A, latch 82 represents the output of the latch 82 in Fig. 12, and the latches 85 and 86 represent the video data that are latched and that, via the switch 83, are output to the LCD source driver 31. As is shown in Fig. 13B, when the first video data is received following the issue of the video data transmission start command (Cmd Video), the one pulse signal SPin is output. That is, the state is shifted from 0 to 1. Also, the signal STB is set to 1 upon the receipt of a strobe ON command (Cmd StbOn), and is cleared upon the receipt of a strobe OFF command (Cmd StbOf). In addition, upon the receipt of the output polarity designation command (Cmd Pos/Cmd Neg), the signal POL is shifted to a bit that represents the designated polarity. In this embodiment, the controller 88 is operated at 1/28 of the input clock.

**IN THE CLAIMS**

Please amend Claims 1, 4, 6, 10, 12 and 14 as set forth below.

--1. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and a driver for applying a voltage to said liquid crystal cell based on an input video signal, wherein

said driver includes a plurality of driver ICs that are mounted on said substrate and are cascade-connected in series using signal lines.

Sub B2

4. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of driver ICs chain-connected in series using signal lines, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said driver distributes said video signal to said plurality of driver ICs with providing a masking signal from an upstream driver IC to a downstream driver IC of said plurality of driver ICs, wherein said masking signal masks said video signal to be provided by said upstream driver IC.

Sub B3

6. (Once Amended) A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of driver ICs that are cascade-connected, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said plurality of driver ICs of said driver are cascade-connected in series by a video transmission line provided on said substrate, and are controlled by serial data that are transmitted along said video transmission line.

Sub B4

10. (Once Amended) A liquid crystal controller comprising:

a receiver for receiving a video signal from a host to display an image;

a sequencer for, upon the receipt of a control signal from said host, generating header information for packet data that are to be output to an LCD driver comprising a plurality of driver ICs which are cascade-connected in series; and

output means for converting said video signal received from said receiver into a serial video signal, for adding said header information generated by said sequencer to said serial video signal, and for outputting the resultant serial video signal to the ICs of said LCD driver.

Sub B5

12. (Once Amended) A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs, comprising the steps of:

transmitting a video signal, including a horizontal blanking period, to said driver ICs in series via a serial interface; and

transmitting a synchronization pattern during said horizontal blanking period in order to synchronize said video signal for said driver ICs.

Sub B6

14. (Once Amended) A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs that are cascade-connected, comprising the steps of:

transmitting a video signal via a serial interface to said driver ICs that are cascade-connected in series; and

applying to an LCD a voltage based on said video signal that is received and that is to be processed by each of said driver ICs;